Multi-Drop LVDS with Virtex-E FPGAs

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Summary

This application note describes how to use LVDS signaling for high-performance multi-drop applications with Virtex-E FPGAs. Multi-drop LVDS allows many receivers to be driven by one Virtex-E LVDS driver. Simulation results indicate that the reference design described here will operate from DC up to 311 Mbits/s. This application note includes DC specifications, microstrip and layout guidelines. With simple source and differential termination, Virtex-E FPGAs drive multi-drop LVDS directly, replacing costly TTL-LVDS drivers and receivers, reducing board area and skew for high-performance applications. The Virtex-E driver actually improves signal integrity over other LVDS drivers by absorbing any reflected energy at the source instead of passing it on down the line. This innovation enables 311 Mb/s signaling on multi-drop lines with as many as 20 LVDS receivers, spanning distances of over four feet in the reference design, with high signal integrity and noise immunity.

Introduction

LVDS uses differential signaling to increase noise immunity over single-ended techniques. Multi-drop LVDS allows many receivers to be driven by one Virtex-E LVDS driver. The true differential LVDS input and output capability of the Virtex-E FPGA enables this multi-drop application. Virtex-E multi-drop LVDS drivers can drive lines with fanouts of 20 to 1, making Virtex-E LVDS suitable for a broad variety of high-load applications. The Virtex-E LVDS driver eliminates costly TTL-LVDS translators, enabling the direct interface of logic to high-speed differential signaling. This integration reduces signal skew and reduces the board area needed to implement a high-performance application.

Multi-Drop LVDS Circuits

Figure 1 shows a typical multi-drop LVDS application. The Q and $\overline{Q}$ outputs of the LVDS driver on the left connect serially to the inputs of the LVDS receivers along the length of the multi-drop lines. A resistor R_T terminates the Q and $\overline{Q}$ signals in parallel at the end of the multi-drop lines. Simple microstrip lines made on standard PC boards with ground planes suffice for this application.

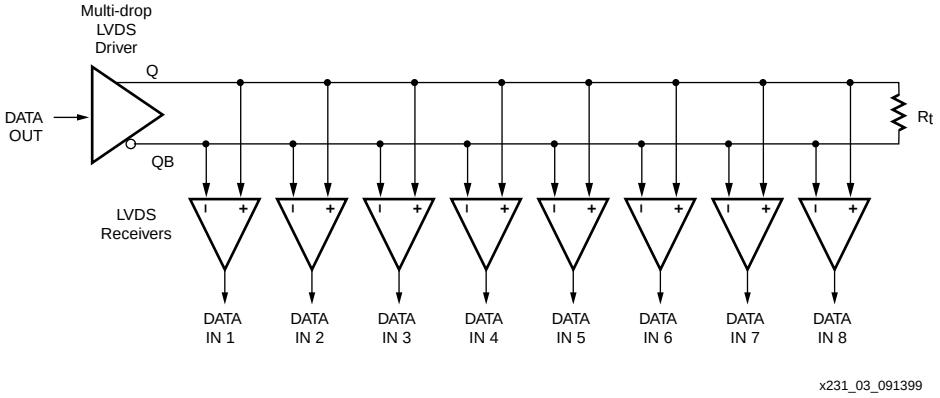


Figure 1: Typical Multi-Drop LVDS Application

Microstrip Transmission Lines for Multi-Drop LVDS

Microstrip is a PCB (printed-circuit board) trace on the top or bottom layer of the PCB over a ground or power plane on the next inner layer. Figure 2 shows the cross-section of a microstrip transmission line. The trace width (w), trace height above ground plane (h), trace thickness (t), and the relative dielectric constant (ε_r) of the PCB determines the microstrip characteristic impedance (Z_0). Table 1 summarizes the characteristic impedance of the microstrip in Figure 2 for typical values of w and h on an FR4 PCB using 1 ounce copper.

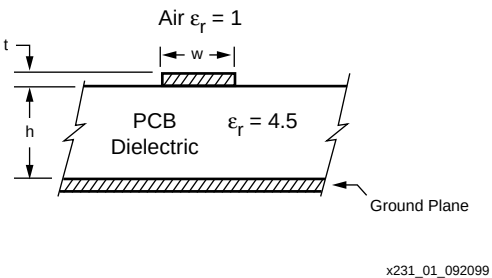


Figure 2: Microstrip Transmission Line Cross-Section

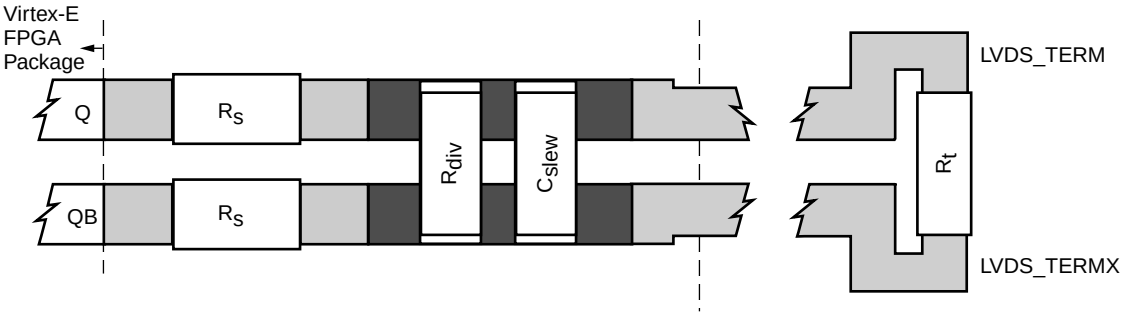
Table 1: Microstrip Impedance for Typical Values of w and h.

Trace Width (w) Mils	Height Above Plane (h) Mils	Impedance (Z_0) Ohms
4	5	70
6	5	59
8	5	51
16	10	52
16	5	34
20	5	29
40	10	30
40	5	17

Notes:
t = 1.4 mils (1 ounce copper)
ε_r = 4.5 (typical FR4 at high frequencies)
1000 mils = 1 inch = 25.4 mm
Impedence error = ± 2%

Trace widths and heights above the plane are rounded to the nearest mil for ease of layout and fabrication. Note the microstrip transmission line impedance is approximately constant with the w/h ratio. A w/h ratio of four, gives approximately Z_0 = 29 to 30 ohms. A w/h ratio of 1.6, gives approximately Z_0 = 51 to 52 ohms. Using the w/h ratio approximation, the characteristic impedance of a microstrip with any plane spacing can be estimated.

Figure 3 is a sample layout of the Virtex-E multi-drop LVDS driver with source resistors and capacitor on the left, and the termination resistor on the right.



Notes:
1. All PCB traces shown are 29Ω microstrip.
2. Can use higher impedance in series with R_S and R_{div}

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Figure 3: Physical Layout of Virtex-E Multi-Drop LVDS Driver

Multi-Drop LVDS DC Specifications

LVDS outputs typically drive a ± 350 mV voltage swing (Q - $\overline{Q}$), and the average of Q and $\overline{Q}$, (Q + $\overline{Q}$) /2, is sometimes referred to as the offset voltage or common-mode voltage. Typical LVDS output common-mode voltage is 1.25 V, and is set by the LVDS driver. For more information on multi-drop LVDS, read National Semiconductor's application note AN-1115, located at http://www.national.com/an/AN/AN-1115.pdf. Table 2 summarizes the DC specifications of LVDS.

Table 2: Standard LVDS DC Specifications

DC Parameter	Conditions	Min	Typ	Max	Units
Output High Voltage for Q and $\overline{Q}$	R_T across Q and $\overline{Q}$ signals	–	1.38	1.6	V
Output Low Voltage for Q and $\overline{Q}$	R_T across Q and $\overline{Q}$ signals	0.90	1.03	–	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), Q = Low	R_T across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage (Q + $\overline{Q}$)/ 2	R_T across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High ($\overline{Q}$ - Q), Q = Low	Common-mode input voltage = 1.25V	100	350	–	mV
Input Common-Mode Voltage (Q + $\overline{Q}$)/ 2	Differential input voltage = ± 350 mV	0.25	1.25	2.25	V

Driving Multi-Drop LVDS from Virtex-E Devices

Figure 4 shows the complete schematic of the Virtex-E LVDS line driver driving 20 LVDS receivers in a multi-drop configuration. The receivers are either Virtex-E receivers or other off-the-shelf LVDS receivers. The LVDS signal is driven from a Virtex-E LVDS driver on the left, and is daisy-chained with two 29-ohm transmission lines and stubs to all 20 LVDS receivers at the OUT[1:20] and $\overline{OUT[1:20]}$ nodes. Each LVDS receiver taps off the main multi-drop lines every 2.5 inches for a multi-drop line length of 50 inches. Each LVDS receiver tap line has a one inch maximum stub length with a 50-ohm transmission line impedance to ground, or a differential impedance of 100 ohms between the two stubs. A 44-ohm termination resistor R_T is placed across the LVDS_TERM and $\overline{LVDS\_TERM}$ nodes close to the final LVDS receiver, on the right. Resistors R_S and R_{DIV} attenuate the signals coming out of the Virtex-E LVDS drivers with V_{CCO} = 2.5V and provide a 22-ohm source impedance (series termination) to the 29-ohm transmission lines. The design calls for a 22-ohm source impedance because the added load of the LVDS receivers brings the 29-ohm line down to an effective impedance of 22 ohms on average. The capacitor C_{SLEW} reduces the slew rate from the Virtex-E LVDS driver, resulting in smaller reflections and less ringing at the receivers.

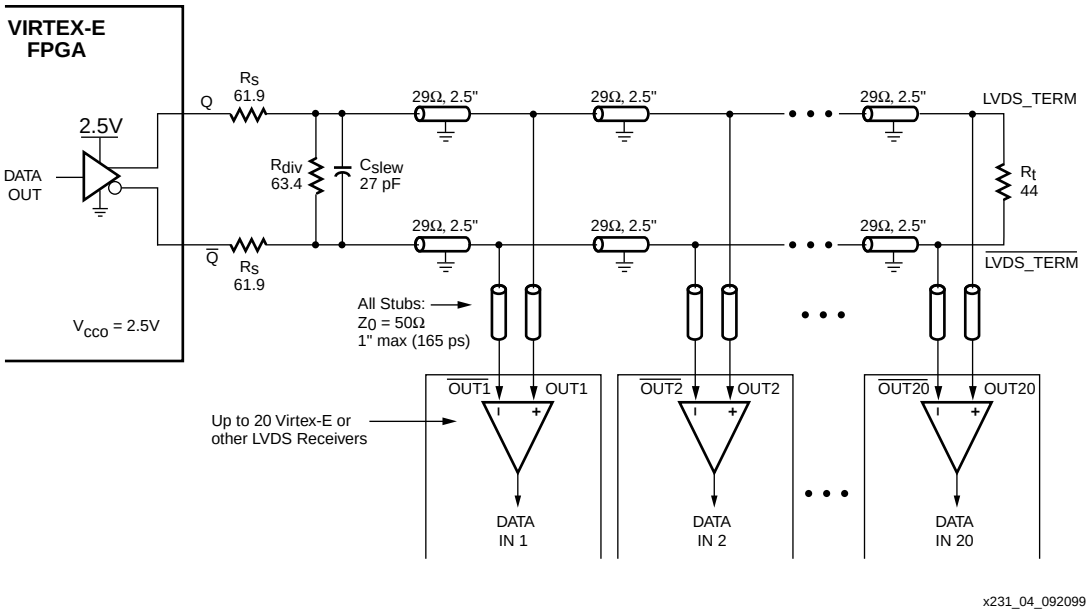

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Figure 4: Virtex-E 20-Load Multi-Drop LVDS Schematic

Why would a 29-ohm transmission line be terminated at both ends with 22 ohm terminations? The answer lies in the behavior of transmission lines. When capacitive receivers and stubs load down a transmission line, the extra capacitance reduces the effective impedance. The receivers in Figure 4 have an effective load capacitance of roughly 9 pF, including receiver capacitance, trace and stub capacitance. A 9 pF capacitor placed every 2.5 inches on a 29 ohm line brings the line down to 22 ohms. Therefore, the reflections are minimized if the line is terminated into 22 ohms. For further information on effective transmission line impedance, see Howard W. Johnson, "High-speed digital design: a handbook of black magic," 1993, pp. 172-174. The section on equally-spaced capacitive loads provides the following equations:

If $Z_0 = \sqrt{L/C}$

where L = inductance / unit length

C = capacitance / unit length

and C_L = capacitance of each load

N = number of loads

H = total length of transmission line

Then $Z_{0EFF} = \sqrt{L / [C + N*C_L/H]}$

Although the transmission line uses lower impedance than the typical impedance found in the specification used in Table 2, all the voltage swings comply with the LVDS standard. This means that any LVDS receiver will work correctly on this multi-drop line. In fact, the lower impedance results in a wider

trace, reducing inductance and skin-effect losses along the multi-drop lines. The two 29-ohm single-ended transmission lines can be microstrip, stripline, or the single-ended equivalent of a 58-ohm twisted pair or similar balanced differential transmission line. See Appendix A in Xilinx application note XAPP230, "The LVDS I/O Standard" for a discussion of transmission lines and terminations used in LVDS.

The multi-drop Virtex-E LVDS line driver adheres to all the standard ANSI/TIA/EIA-644 LVDS Interface Standard DC input levels as specified in Table 2. The output common-mode voltage typically averages to $V_{CCO}/2$. Component value derivations for R_S, R_{DIV}, and C_{SLEW} can be found in Appendix B on page 10. The DC performance of Virtex-E LVDS meets or exceeds the ANSI/TIA/EIA-644 LVDS Interface Standard specifications shown in Table 2.

The Virtex-E multi-drop LVDS termination in Figure 4 differs from other LVDS source terminations in that it actually absorbs reflected energy at the source. While most LVDS drivers behave like a current source with a high output impedance, the Virtex-E multi-drop LVDS line driver behaves like a current source in parallel with a 22-ohm resistor, thereby improving the source termination for reflected signals. The 22-ohm source impedance of the Virtex-E LVDS driver absorbs nearly all differential reflections from the capacitive loads distributed along the multi-drop lines, reducing standing waves, undershoot, and noise levels compared to other LVDS drivers. The voltages at LVDS_TERM and $\overline{\text{LVDS\_TERM}}$ and on the transmission lines meet or exceed all of the standard LVDS output levels shown in Table 2.

Figure 5 shows the typical step response of Virtex-E multi-drop LVDS drivers for the schematic in Figure 4. The top graph shows the single-ended waveforms at outputs 1, 10, and 20, corresponding to receivers at the beginning, middle, and end of the multi-drop line. The bottom graph shows the differential voltage at five receivers along the multi-drop line from beginning to end. All voltages are measured at the on-die differential input of the receiver. All received waveforms show similar characteristics with little undershoot or overshoot and negligible load reflections.

Figure 6 shows typical 311 Mb/s burst data (or 155.5 MHz clock) response of Virtex-E multi-drop LVDS outputs for the schematic in Figure 4. Single-ended and differential waveforms are shown for outputs 1, 10, and 20 along the multi-drop line. All received waveforms show similar characteristics with little or no undershoot/overshoot and negligible reflections. Some smoothing of the waveform occurs over the length of the multi-drop line loaded by the receivers, but the attenuation is minor. Even the last receiver sees nearly 400 mV peak at the end of the 50 inch line after 19 other receivers. The excellent performance of Virtex-E multi-drop LVDS can be attributed to its matched source impedance and the rise-time-reducing capacitor C_{SLEW} at the source.

The Virtex-E multi-drop LVDS driver is fully compatible with LVDS receivers from National Semiconductor and other companies.

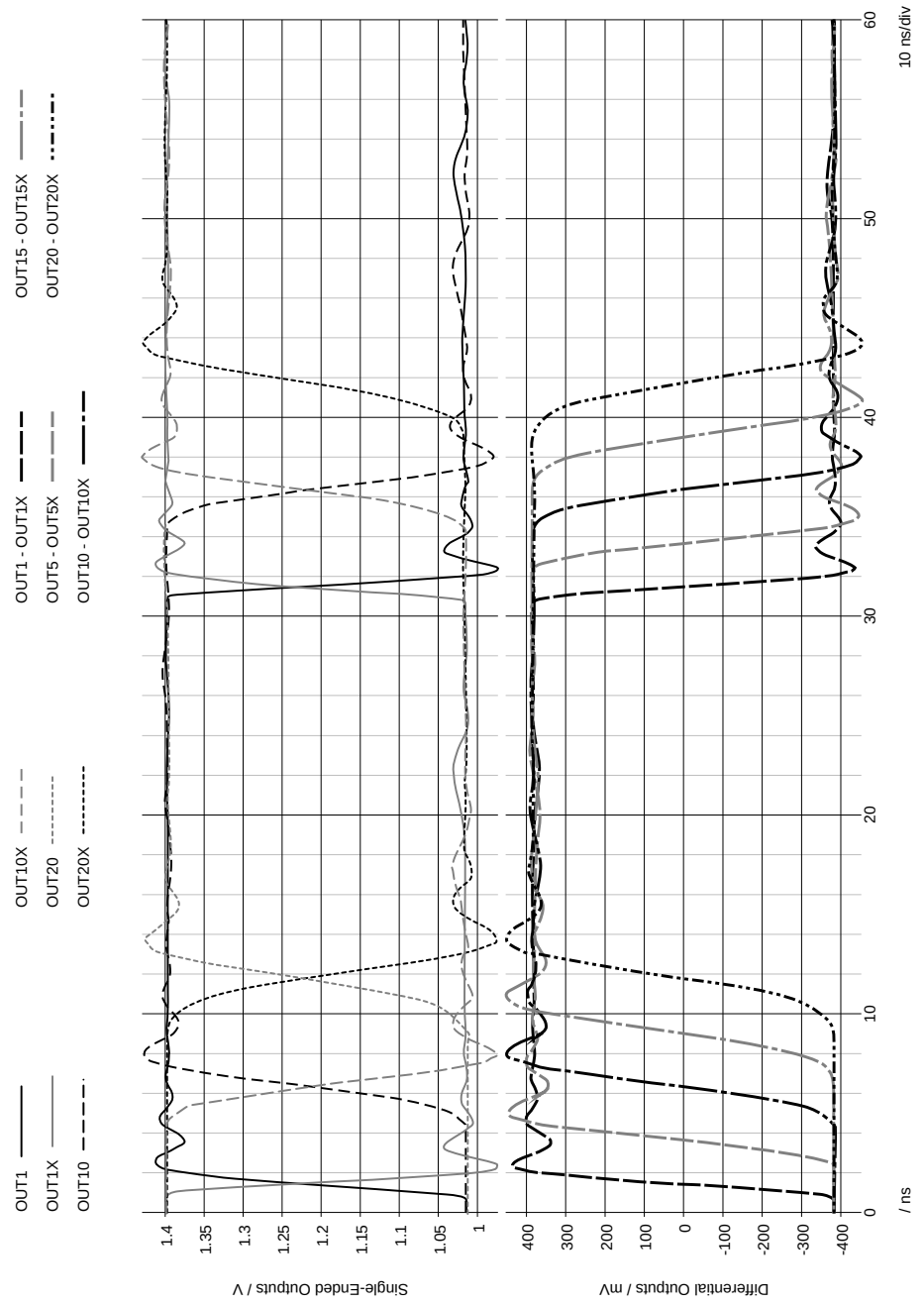

Figure 5: Typical Step Response of Virtex-E Multi-drop LVDS Drivers

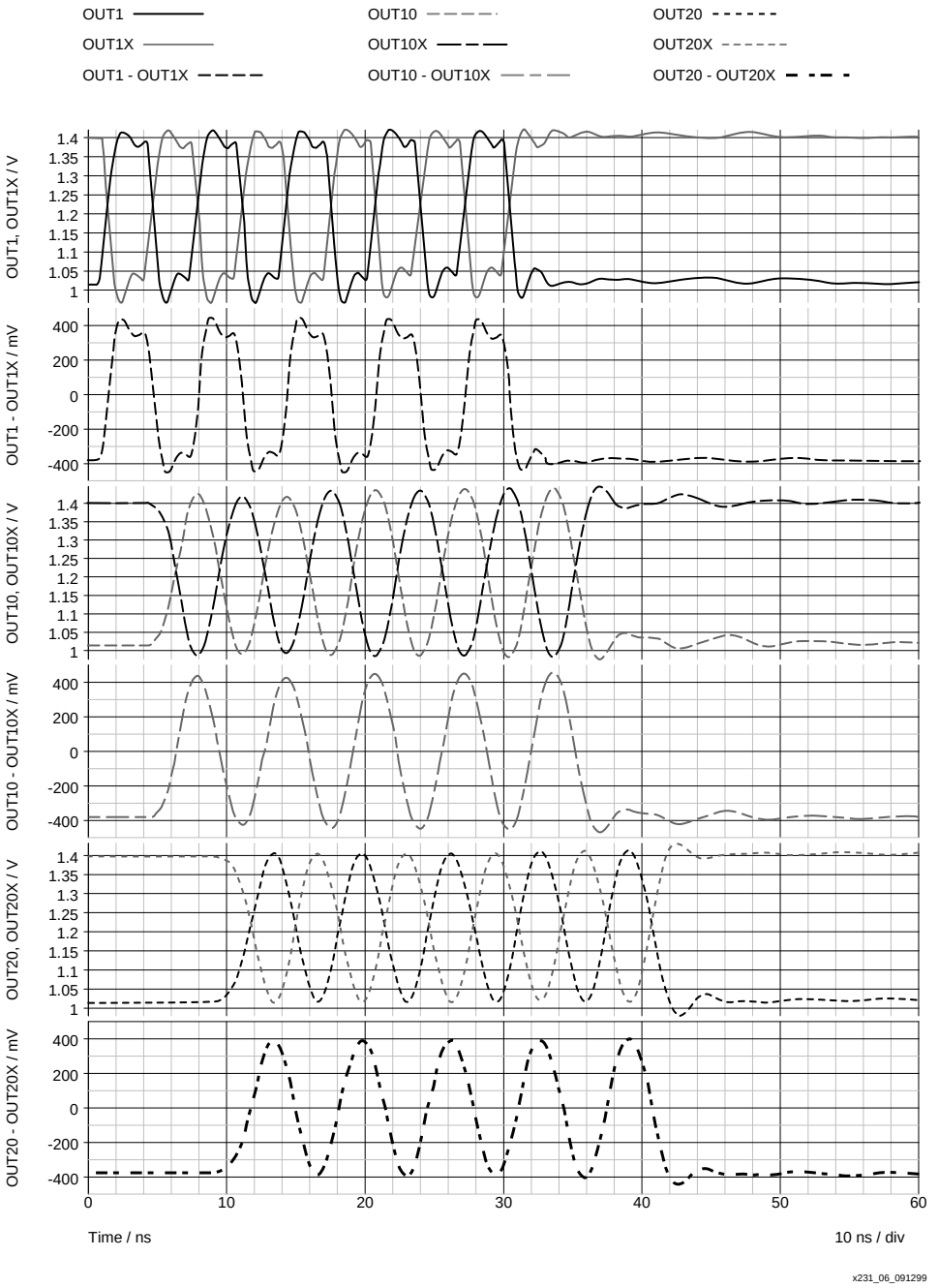

Figure 6: Typical 311 Mb/s Burst Data Response for Virtex-E Multi-drop LVDS Output for Schematic in Figure 4.

Conclusion

The Virtex-E FPGA transmits and receives multi-drop LVDS. The maximum data rate is 311 Mb/s or a clock of 155.5 MHz for the -7 Virtex-E speed grade. Virtex-E LVDS drivers provide significant improvement in signal integrity over other off-the-shelf LVDS drivers due to their matched source impedance which series terminates the transmission lines and minimizes source reflections. Reliable data transmission is possible for up to 20 LVDS receivers over electrical lengths of 8.25 ns (50 inches), limited only by skin effect losses in the PCB trace. Virtex-E FPGAs utilizing LVDS eliminate costly TTL-LVDS drivers and LVDS-TTL receivers, reduce board area, and reduce signal delay skew, while reliably transferring high-speed data and clocks over long distances between chips, boards, chassis, and peripherals.

Appendix A: PCB layout guidelines for Virtex-E multi-drop LVDS

Printed-circuit board layout guidelines for the Virtex-E multi-drop LVDS circuit in Figure 4 are as follows:

1) A multi-layer printed-circuit board with controlled transmission line impedances is required.

2) All transmission lines between LVDS drivers and receivers should be referenced to a common ground plane except when routed through a balanced differential transmission line such as twisted-pair. For twisted-pair and other balanced lines, utilize a grounded shield that connects to the ground planes at the beginning and ending of the twisted-pair cable to allow for common-mode return current. If no shield connection is available, take extra care to use symmetric and equal-length routing and ensure capacitive load balancing on the differential pair to prevent excessive common-mode to differential mode conversion. Do not split the ground plane under the signal path as this will cause large discontinuities from increased inductance.

3) The resistors R_S and R_{DIV} should be placed close to the Virtex-E outputs for the Virtex-E multi-drop LVDS line driver. Place the parallel termination resistor R_T close to the final LVDS inputs at the far end of the multi-drop line.

4) The capacitor C_{SLEW} should be placed close to resistors R_S and R_{DIV}.

5) Symmetric and equal-length routing should be used of the multi-drop LVDS signal pair between source and destinations to maximize common-mode rejection. Route the two LVDS signals with minimal spacing between the traces along the multi-drop line and the stubs. If the trace spacing is less than the dielectric thickness to the ground plane, differential impedance effects must be included to determine the effective transmission line impedance since the trace impedance will be significantly affected by the differential impedance between the two traces. Wider spacing has a smaller effect on the impedance.

6) Virtex-E provides dedicated LVDS input/output pairs for driving and receiving LVDS. The IOB registers driven from a single clock provide a convenient point to synchronize inputs and outputs.

Appendix B: Component value derivations for the Virtex-E multi-drop LVDS line driver

Referring to Figure 4, resistors R_S and R_{DIV} attenuate the signals coming out of the Virtex-E LVDS drivers and provide a matched source impedance (series termination) to the transmission lines. Values for R_S and R_{DIV} are determined by these two constraints. The equivalent source impedance R_{EQ}, including the Virtex-E driver impedance R_{DRIVER}, must equal the effective transmission line impedance, 22 ohms. Using the differential half-circuit:

$$(R_{DIV} \rightarrow R_{DIV}/2,\ R_T \rightarrow R_T/2),$$
$$R_{EQ} = (R_{DRIVER} + R_S) \,//\, (R_{DIV}/2) = Z_{0EFF} \qquad (1)$$

R_S and R_{DIV} are chosen to obtain the desired attenuation of the signal path from the Virtex-E driver to the LVDS destinations. The desired signal attenuation is defined as α.

$$\alpha = V_{SWING}(LVDS) / V_{CCO} = [(R_{DIV}/2) / (R_{DIV}/2) + R_{DRIVER} + R_S)]\ [R_T/2 / (R_T/2 + R_{EQ})]$$

$$R_T/2 / (R_T/2 + R_{EQ}) = 1/2, \text{ therefore,}$$
$$\alpha = V_{SWING}(LVDS) / V_{CCO} = [(R_{DIV}/2) / (R_{DIV}/2) + R_{DRIVER} + R_S)] / 2 \qquad (2)$$

Using equations 1 and 2 and solving for R_{DIV} and R_S yields:

$$R_S = (Z_{0EFF} / 2\alpha) - R_{DRIVER} \qquad (3)$$
$$R_{DIV} = [4\alpha / (1 - 2\alpha)]\ [R_{DRIVER} + Rs] \qquad (4)$$

Substituting Z_{0EFF} = 22 ohms, R_{DRIVER} = 10 ohms, V_{CCO} = 2.5V, and $V_{SWING}(LVDS)$ = 380 mV into Equations 2 - 4 and rounding to the nearest 1% value, the values of R_S = 61.9 ohms and R_{DIV} = 63.4 ohms are found, shown in Figure 4. The typical LVDS voltage swing of 350 mV is increased to 380 mV to offset skin effect losses at 311 Mb/s data rates near the end of the 50-inch multi-drop lines.

C_{SLEW} increases the rise time out of the Virtex-E multi-drop driver. Typically, the 10-90% rise time of LVDS is 500 ps. Using C_{SLEW}, the desired rise time is increased to approximately 1 ns. Using the differential half-circuit equivalent of Figure 4, ($R_{DIV} \rightarrow R_{DIV}/2$, $C_{SLEW} \rightarrow 2C_{SLEW}$), the driving point impedance for $2C_{SLEW}$ is $R_{EQ} \,//\, R_T/2 = R_{EQ}/2$. The RC time constant is:

$$(2C_{SLEW})(R_{EQ}/2) = R_{EQ}\ C_{SLEW}.$$

By setting τ, the RC time constant, equal to the original LVDS 10-90% rise time, the new 10-90% rise time will be nearly 1 ns. The value for C_{SLEW} is calculated as:

$$C_{SLEW} = \tau / R_{EQ} \qquad (5)$$

Substituting τ = 500 ps and R_{EQ} = 22 ohms into Equation 5 and rounding up to the nearest 10% value, the value of C_{SLEW} = 27 pF is obtained, shown in Figure 4.

Revision History

Date	Version	Revision
9/23/99	1.0	Initial Xilinx release